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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/814,867	03/30/2004	Frederic J. Bernard	IMPJ-0031	5627

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EXAMINER

TON, MY TRANG

ART UNIT	PAPER NUMBER
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2816

DATE MAILED: 05/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/814,867

Applicant(s)

BERNARD ET AL.

Examiner

My-Trang N. Ton

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 02 March 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-100 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 1-89 and 96-100 is/are allowed.
- 6) ☒ Claim(s) 90 and 91 is/are rejected.
- 7) ☒ Claim(s) 92-95 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 18 January 2006 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.


MY-TRANG NUTON
PRIMARY EXAMINER

Attachment(s)

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 03/02/06.
- ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- ☐ Notice of Informal Patent Application (PTO-152)
- ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

The IDS filed on 03/02/06 has been received and considered.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 90-91 are rejected under 35 U.S.C. 102(b) as being anticipated by Kobatake (U.S Patent 5,729,155).

Kobatake discloses in Fig. 5A a voltage level shift circuit including:

a first and a second pFET (P21, P23) each having a source, drain, well and gate terminal, the source and well of each coupled to a high-voltage supply (V_{pp}), the drain of the first PFET (P23) coupled to a first intermediate node (G) and its gate coupled to a second intermediate node (E), the drain of the second pFET (P21) coupled to the second intermediate node (E) and its gate coupled to the first intermediate node (G);

a third and fourth PFET (P22, P24), the third PFET (P24) having its source coupled to the first intermediate node (G), its drain coupled to a first of two complementary switched voltage output nodes (OUT21) and its gate coupled to an intermediate-voltage supply (V_{MP}), and the fourth PFET (P22) having its source coupled to the second intermediate node (E), its drain coupled to the second of two

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complementary switched voltage output nodes (OUT21*) and its gate coupled to the intermediate-voltage supply (VMP); and

a first and a second high-voltage circuit portion (N21-N24), the first high-voltage circuit portion (N24, N23) coupling the first (OUT21) of two complementary switched voltage output nodes to a ground (Ground) through a circuit element (N23) responsive to the Reset signal (is seen to defined intended use, IN2* reads on Reset signal), the second high-voltage circuit portion (N22, N21) coupling the second (OUT21*) of two complementary switched voltage output nodes to the ground (GROUND) through a circuit element (N21) responsive to the Set signal (is seen to defined invented use, IN2 reads on Set signal) as recited in claim 90.

Regarding claim 91: the first and second high-voltage circuit portion (N21-N24) comprise:

a first and a second high-voltage nFET (N22, N24), the first high-voltage nFET (N24) having its drain coupled to the first (OUT21) of two complementary switched voltage output nodes, its gate coupled to a Vdd supply (VMN), and its source coupled to the ground (ground) through a first transistor (N23) responsive to the Reset signal (IN2*), the second high-voltage nFET (N22) having its drain coupled to the second (OUT21*) of two complementary switched voltage output nodes, its gate coupled to the Vdd supply (VMN), and its source coupled to ground (GROUND) through a second transistor (N21) responsive to the Set signal (IN2).

Allowable Subject Matter

Claims 1-89, 96-100 are allowable over the prior art of record.

Claims 92-95 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to My-Trang N. Ton whose telephone number is 571-272-1754. The examiner can normally be reached on 7:00 a.m - 5:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



My-Trang N. Ton
Primary Examiner
Art Unit 2816

May 08, 2006